REMARKS/ARGUMENTS

Favorable reconsideration of this application as presently amended and in light of the following discussion is respectfully requested.

Claims 2-17 are pending in the present application. Claims 2-6 are amended, Claim 1 is canceled, and Claims 12-17 are added by the present amendment.

Claim amendments and new claims find support in the specification and claims as originally filed at least at Figures 2 and 11, and at page 20, line 21, to page 21, line 2. Thus, no new matter is added.

In the outstanding Office Action, Claims 2 and 3 were objected to; Claims 1-4 and 6 were rejected under 35 U.S.C. § 103(a) as unpatentable over Akiyama et al. (herein "Akiyama") in view of U.S. Publication No. 2001/0040255 to Tanaka; Claim 5 was rejected under 35 U.S.C. § 103(a) as unpatentable over Akiyama in view of Tanaka and U.S. Patent No. 6,798,040 to Reznik; and Claims 1, 2, 3 and 6 were rejected under 35 U.S.C. § 103(a) as unpatentable over Tanaka.

Initially, Applicants and Applicants' representative gratefully acknowledge the courtesy of a personal interview with Examiner Landau on October 25, 2005. During the interview, differences between the claimed invention and references in the Office Action were discussed. In particular, Examiner Landau agreed that the references in the outstanding Office Action do not teach or suggest a substrate having a thickness of 200 μm or less, and having the particular coverage of first and second semiconductor layers on a second electrode of an insulated gate bipolar transistor. Comments discussed during the interview are reiterated below.

Regarding the objection to the claims, Claims 2 and 3 are amended to more clearly recite the invention as suggested in the outstanding Office Action. Accordingly, it is respectfully requested that objection be withdrawn.

Applicants respectfully traverse the rejection of Claims 1-4 and 6 under 35 U.S.C. § 103(a) as unpatentable over Akiyama and Tanaka, with respect to amended Claim 2 and 3.

Amended Claim 2 is directed to an insulated gate bipolar transistor including, *inter alia,* a semiconductor substrate of a first conductivity type including a first main surface and a second main surface, an insulated gate transistor formed in a region of the semiconductor substrate and including a channel of the first conductivity type which is formed within a base region of a second conductivity type during an on state of the insulated gate transistor. The base region extends from the first main surface toward an interior of the semiconductor substrate. The insulated gate bipolar transistor also includes a first main electrode formed on the first main surface and in contact with the base region of the insulated gate transistor at the first main surface, first and second semiconductor layers of the first and second conductivity types, respectively, formed on the second main surface of the semiconductor substrate and facing the insulated gate transistor, and a second main electrode formed on the first semiconductor layer and the second semiconductor layer.

Further, Claim 2 includes a first interface between the first semiconductor layer and the second main electrode that occupies 20-70% of the interface between the second main electrode and each of the first and second semiconductor layers, and alternatively, Claim 3 includes a first interface between the first semiconductor layer and the second main electrode that occupies 20-70% of the interface between the second main electrode and each of the first and second semiconductor layers.

As discussed during the interview, the combined disclosures of Akiyama and Tanaka do not teach or suggest each of the features of amended Claims 2 and 3. Akiyama describes a structure comprising an N-type layer and a P-type layer, each of which has a thickness of 30 μm and is provided on a back surface, and an N^- - type layer with a thickness of 190 μm. In other words, Akiyama describes a substrate having a thickness of 220 μm. Tanaka indicates

that a thickness of each of an N- type layer and a P-type layer formed on a back surface is equal to 1 μm or smaller, but does not indicate any thickness of an N^--type layer.

On the other hand, Claims 2 and 3 of the present application are directed to an insulated gate bipolar transistor in which a thickness of an N^--type layer is from 50 μm to 500 μm, and a thickness of each of an N-type layer and a P-type layer formed on a back surface is equal to 2 μm or smaller. Further, Claims 2 and 3 recite an optimal solution of a ratio of the portion of the interface with the second electrode occupied by N-type and P-type layers formed on the back surface, as obtained by Applicants simulations described in the specification, to achieve the stated advantages. That is, Claims 2 and 3 reflect the results of simulations carried out under conditions including the thickness of the substrate, and show that the situation that a ratio of the above N-type layer and P-type layer formed on the back surface within a range specified in Claims 2 and 3 is optimal. Applicants submit the features of Claims 2 and 3 described above are not suggested by the disclosures of Akiyama and Tanaka because Claims 2 and 3 are directed to inventions based on results obtained for the first time by carrying out simulations under the above conditions.

Further, as discussed during the interview, even if the 1 μm or smaller P-type and N-type regions of Tanaka were combined with the 220 μm substrate of Akiyama (i.e., 30 μm thick N-type and P-type layers, plus 190 μm thick N^-- type layer), neither reference indicates it would be necessary for a resulting combination to include a substrate having a thickness of less than 200 μm. For example, a combination of these features may result in a substrate as described by Tanaka having a thickness of 220 μm, but including 1 μm thick P-type and N-type layers, as described by Akiyama. A reference is good for only what it clearly and definitely discloses, In re Moreton, 129 USPQ 227, 230 (CCPA 1961).

It is well recognized that in order to have a valid case of *prima facie* obviousness, all claim limitations must be taught or suggested (see MPEP §2143). As no proper *prima facie*

obviousness has been established, as noted above, the rejection of independent Claim 1, with respect to amended independent Claims 2 and 3, is also traversed for the reasons set forth above.

Accordingly, Applicants respectfully submit that independent Claims 2 and 3, and claims depending therefrom, patentably define over Akiyama and Tanaka.

Further, Applicants respectfully traverse the rejection of Claim 5 under 35 U.S.C. § 103(a) as unpatentable over Akiyama in view of Tanaka and Reznik.

First, Applicants traverse the assertion in the outstanding Office Action that it would have been obvious to the ordinary artisan at the time the invention was made to modify the invention of Akiyama by including the additional semiconductor layer of Reznik for the purpose of elevating the charge carrier density in the region.[1] Applicants respectfully submit that the advantages asserted in Reznik are directed to an invention having incompatible goals with the present invention, and therefore one of skill in the art would not have been motivated to combine those features with the invention of Akiyama. In particular, Reznik describes a power semiconductor switch including successive regions whose conductivities have alternating signs for the purpose of producing a symmetrically blocking switch that blocks current in the opposite direction up to high voltages. However, the claimed invention relates to an insulated gate bipolar transistor including a built in freewheeling diode to cause current to flow through the integrated gate bipolar transistor through a bypass path during an off state. Further, the power semiconductor switch of Reznik includes a buffer layer 2 and a further doped region 3 that are not found in the present invention. Accordingly, Applicants respectfully submit that one of skilled in the art would not have been motivated to combine the features described by Reznik with the features described by Akiyama because the purposes of those disclosures are incompatible.

[1] Office Action at page 6, lines 8-12.

In addition, as discussed above, Claim 2 is believed to patentably define over Akiyama and Tanaka, and Claim 5 depends from Claim 2. Further, Applicants respectfully submit that Reznik does not supply the claimed features lacking in the disclosure of Akiyama and Tanaka. Accordingly, for that reason as well as the reason described above, Applicants respectfully request the rejection of Claim 5 be withdrawn.

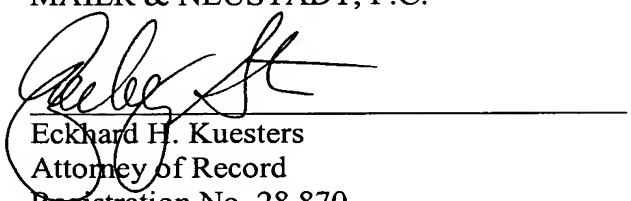
Further, Applicants respectfully note that none of the references cited in the outstanding Office Action teach or suggest the features of new Claims 12-17 for reasons similar to those described above.

Accordingly, Applicants respectfully submit that independent Claims 2 and 3, and claims depending therefrom, are allowable.

Consequently, in light of the above discussion and in view of the present amendment, the present application is believed to be in condition for allowance and an early and favorable action to that effect is respectfully requested.

Respectfully submitted,

OBLON, SPIVAK, McCLELLAND,
MAIER & NEUSTADT, P.C.



Eckhard H. Kuesters
Attorney of Record
Registration No. 28,870

Zachary S. Stern
Registration No. 54,719

Customer Number
22850

Tel: (703) 413-3000
Fax: (703) 413 -2220
(OSMMN 06/04)

EHK:ZSS:dnf

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